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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,162	11/17/2003	Shiro Dosho	60188-706	9457

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EXAMINER	
NGUYEN, MINH T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 01/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,162	DOSHO ET AL.	
	Examiner	Art Unit	
	Minh Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 and 6-8 is/are rejected.

7)☒ Claim(s) 5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 17 November 2003 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 11/17/03.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1, 4, 6 and 8 are objected to because of the following informalities:

In claim 1, last line, "the received signal" should be changed to -- the first clock signal -- to avoid potential antecedent basis problem.

In claim 4, line 2, "a received signal and which receives" should be deleted to avoid potential antecedent basis problem.

In claim 6, line 8, "tuned on" should be changed to -- turned on --.

In claim 8, the same problem exists as discussed in claim 6.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 6 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 6, the recitation on the last seven lines is unclear and confusing. Specifically, the phrase "the transistor forming the delay unit has either one of the n- and p-channel types in respect of which type transistors included in the clock-signal production circuit

and in the first output unit of the clock-signal output circuit" is unclear and appears redundant. Clarification is requested. The phrase "turned on when the third clock signal transitions to the first logic output value are different in number from transistors included in the clock-signal production circuit and in the second output unit of the clock-signal output circuit and turned on when the third clock signal transitions to the second logic output value" appears misdescriptive because the transistor in the delay unit is always ON (configured as a diode, see claim 5), i.e., it cannot be turned ON or OFF as recited. Clarification is requested.

As per claim 8, the same problem exists as discussed in claim 6.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-4 and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,488,317, issued to Webster et al.

As per claim 1, Webster discloses a duty cycle correction circuit (Fig. 3) comprising:

a delay unit (transistors 34 and 36) for receiving a first clock signal (at the I/O node) in which a first logic value has a shorter period of time per cycle than a second logic value (the structural of the claimed delay unit is not distinguishable from the structural of the Webster's delay unit based on this recited limitation, MPEP 2114. It is clear that the Webster's delay unit is able to receive a clock signal with the recited characteristics), delaying the first clock signal, and

outputting a second clock signal which transitions to the second logic value at a timing at which the period of time equivalent to a half cycle has elapsed since the first clock signal transitioned to the first logic value (this limitation is met because the Webster's delay unit is configured to function as a resistor just like the delay unit shown in Fig. 1 of the present invention, see column 4, lines 49-54, i.e., transistors 34 and 36 are ON and compare with the delay unit shown in Fig. 1 of the present invention, i.e., transistors 111 and 112 are configured to be ON); and

a clock-signal output unit (transistors 38 and 40) for outputting a third clock signal (Y) based on the first and second clock signals,

wherein the clock-signal output unit comprises: a first output unit (transistor 39) for setting the third clock signal (Y) at a first logic output value with either one of the first logic value and the second logic value in response to the transition of the first clock signal to the first logic value (for example, a HIGH of the first clock signal at the gate of transistor 38 provides a LOW at node Y); and a second output unit (transistor 40) for setting the third clock signal (Y) at a second logic output value with the other of the first logic value and the second logic value in response to the transition of the second clock signal (at the gate of transistor 40) to the second logic value (for example, a LOW of the second clock signal at the gate of transistor 40 provides a HIGH at node Y), and

the duty cycle correction circuit receives the first clock signal and corrects the duty cycle of the received signal to output the third clock signal (this is merely a function of any duty cycle correction circuit).

As per claim 2, because the recited frequency divider circuit is not part of the duty cycle correction circuit recited in the preamble of claim 1, no patentable weight is given. In other

words, generating the first clock signal to be fed to the duty cycle circuit having the structure recited in claim 1 by any circuit which includes a frequency divider circuit does not result in a structural distinguishable.

As per claim 3, Webster further discloses:

the first output unit includes a first transistor which is of either one of n-channel type and p-channel type and whose gate receives the first clock signal (as shown, transistor 38 is N type),

the second output unit includes a second transistor which is of the other of n-channel type and p-channel type, whose gate receives the second clock signal and whose drain is connected to a drain of the first transistor (as shown, transistor 40 is the other type, i.e., P type, the drain is connected as recited), and

the third clock signal is based on a signal output from the common drain of the first and second transistors (at node Y).

As per claim 4, the Webster's delay unit is a transfer gate (transistors 34 and 36) which passes the first clock signal (I/O) to output the second clock signal (at the gate of transistor 40).

As per claim 7, Webster further discloses:

the delay unit includes a transistor (NMOS 36) whose gate is supplied with a predetermined voltage (VCC, column 4, line 50) and of which either one of a source and a drain receives the first clock signal to output the second clock signal from the other of the drain and the source (as shown in Fig. 3), and

the predetermined voltage supplied to the gate of the transistor is above a gate threshold value in the case where the transistor is an n-channel transistor while the predetermined voltage supplied to the gate of the transistor is below the gate threshold value in the case where the

transistor is a p-channel transistor (this is the condition for an NMOS transistor ON, note: transistor NMOS 36 is ON, column 4, lines 50-51).

As per claim 8, the recited clock signal production circuit is the circuit which produces the signal I/O, because the signal I/O is an internal signal of a logic module of an FPGA (column 3, lines 12-13), the circuit which produces the signal I/O must be implemented using NMOS and PMOS transistors. As discussed herein above, the recited delay unit and clock signal output unit comprise NMOS and PMOS transistors.

Allowable Subject Matter

4. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 5 is allowable because the prior art of record fails to disclose or suggest the inclusion of a transistor in the delay unit having gate and drain connected to each other. There is no suggestion and/or motivation for doing the modification in the Webster reference because doing such a modification would destroy the reference, i.e., destroying the capability of selecting whether VCC or GND would be provided the gates of transistors 34 and 36.

5. Claim 6 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Claim 6 is allowable for the reason noted in claim 5.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

1/4/04

Minh Nguyen
Primary Examiner
Art Unit 2816